

WHAT IS CLAIMED IS:

- 1 1. A memory system, comprising:
2 a memory cell;
3 first and second bitlines operably connected to said memory cell;
4 a write line operably connected to said memory cell; and
5 an equilibration circuit connected to said first and second bitlines, wherein
6 said equilibration circuit is operable to maintain a predetermined
7 equilibrium condition between said first and second bit lines and
8 wherein said equilibration circuit is controlled by a reference voltage.

- 1 2. The memory system according to claim 1, wherein said equilibration circuit is
2 operable to generate an impedance load in said first and second bit lines at a level that
3 allows generation of differential signals in said bit lines.

- 1 3. The memory system according to claim 2, wherein said equilibration circuit
2 comprises first and second pMOS devices in series with said first and second bitlines,
3 respectively, and a third pMOS device connected between said first and second
4 bitlines and wherein the gates of said first, second and third pMOS devices are
5 connected to said reference voltage.

- 1 4. The memory system according to claim 3, wherein said first, second and third
2 pMOS devices operate as resistors in the linear region of MOSFET device operation.

- 1 5. The memory system according to claim 4, wherein the resistance of said first,
2 second and third pMOS devices is determined by the gate-source voltage of said
3 pMOS devices.

- 1 6. The memory system according to claim 5, wherein said write line is operably
2 connected to said memory cell by at least one transfer gate.

- 1 7. The memory system according to claim 6, wherein said transfer gate
2 comprises an nMOS device and wherein said reference voltage is related to the gate
3 drive current of said transfer gate.

1 8. The memory system according to claim 7, wherein said reference voltage is
2 controlled by a reference circuit that is operable to change said reference voltage to
3 compensate for variations in operating characteristics of said first, second and third
4 pMOS devices.

1 9. The memory system according to claim 8, wherein said reference circuit is
2 further operable to change the reference voltage to compensate for variations in the
3 operating characteristics of said nMOS device comprising said transfer gate.

1 10. The memory system according to claim 9, wherein said reference circuit
2 comprises a current mirror.

1 11. A method for controlling operation of a memory system, comprising:
2 storing information in a memory cell;
3 generating a predetermined equilibrium condition between first and second
4 bitlines operably connected to said memory cell using an equilibration
5 circuit connected to said first and second bitlines, wherein said
6 equilibration circuit is controlled by a reference voltage; and
7 controlling the content of information in said memory cell with a write line
8 operably connected to said memory cell.

1 12. The method according to claim 11, wherein said equilibration circuit is
2 operable to generate an impedance load in said first and second bit lines at a level that
3 allows generation of differential signals in said bit lines.

1 13. The method according to claim 12, wherein said equilibration circuit
2 comprises first and second pMOS devices in series with said first and second bitlines,
3 respectively, and a third pMOS device connected between said first and second
4 bitlines and wherein the gates of said first, second and third pMOS devices are
5 connected to said reference voltage.

1 14. The method according to claim 13, wherein said first, second and third pMOS
2 devices operate as resistors in the linear region of MOSFET device operation.

1 15. The method according to claim 14, wherein the resistance of said first, second
2 and third pMOS devices is determined by the gate-source voltage of said pMOS
3 devices.

1 16. The method according to claim 15, wherein said write line is operably
2 connected to said memory cell by at least one transfer gate.

1 17. The method according to claim 16, wherein said transfer gate comprises an
2 nMOS device and wherein said reference voltage is related to the gate drive current of
3 said transfer gate.

1 18. The method according to claim 17, wherein said reference voltage is
2 controlled by a reference circuit that is operable to change said reference voltage to
3 compensate for variations in operating characteristics of said first, second and third
4 pMOS devices.

1 19. The method according to claim 18, wherein said reference circuit is further
2 operable to change the reference voltage to compensate for variations in the operating
3 characteristics of said nMOS device comprising said transfer gate.

1 20. The method according to claim 19, wherein said reference circuit comprises a
2 current mirror.

1 21. A digital processing system, comprising:
2 a datapath module;
3 a control module;
4 an input-output module; and
5 a memory module, wherein said memory module comprises:
6 at least one memory cell;
7 first and second bitlines operably connected to said memory cell;

8 a write line operably connected to said memory cell; and
 9 an equilibration circuit connected to said first and second bitlines,
 10 wherein said equilibration circuit is operable to maintain a
 11 predetermined equilibrium condition between said first and
 12 second bit lines and wherein said equilibration circuit is
 13 controlled by a reference voltage.

1 22. The method according to claim 21, wherein said equilibration circuit is
 2 operable to generate an impedance load in said first and second bitlines at a level that
 3 allows generation of differential signals in said bitlines.

1 23. The method according to claim 22, wherein said equilibration circuit
 2 comprises first and second pMOS devices in series with said first and second bitlines,
 3 respectively, and a third pMOS device connected between said first and second
 4 bitlines and wherein the gates of said first, second and third pMOS devices are
 5 connected to said reference voltage.

1 24. The method according to claim 23, wherein said first, second and third pMOS
 2 devices operate as resistors in the linear region of MOSFET device operation.

1 25. The method according to claim 24, wherein the resistance of said first, second
 2 and third pMOS devices is determined by the gate-source voltage of said pMOS
 3 devices.

1 26. The method according to claim 25, wherein said write line is operably
 2 connected to said memory cell by at least one transfer gate.

1 27. The method according to claim 26, wherein said transfer gate comprises an
 2 nMOS device and wherein said reference voltage is related to the gate drive current of
 3 said transfer gate.

1 28. The method according to claim 27, wherein said reference voltage is
2 controlled by a reference circuit that is operable to change said reference voltage to
3 compensate for variations in operating characteristics of said first, second and third
4 pMOS devices.

1 29. The method according to claim 28, wherein said reference circuit is further
2 operable to change the reference voltage to compensate for variations in the operating
3 characteristics of said nMOS device comprising said transfer gate.

1 30. The method according to claim 29, wherein said reference circuit comprises a
2 current mirror.